Amendments to the Claims:

Please amend claims 1, 6 and 7 as shown in the listing of claims below. This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) A method for providing a next-cycle input sample from a decision feedback equalizer to a symbol decoder using look-ahead computations such that timing contention between the decision feedback equalizer and the symbol decoder is reduced, the method comprising:

(a) computing, during a symbol period, a set of ~~possible~~ values in the decision feedback equalizer and a set of path memory symbols in the symbol decoder, the set of path memory symbols being based on a current input sample; and

(b) selecting, during the symbol period, one of the ~~possible~~ values as the next-cycle input sample based on at least one of a plurality of next-cycle path memory symbols produced from the symbol decoder.

2. (previously presented) The method of claim 1 wherein the symbol decoder uses a trellis code having N states, wherein the decision feedback equalizer provides N next-cycle input samples to the symbol decoder, the N next-cycle input samples corresponding one-to-one to the N sates of the trellis code.

3. (original) The method of claim 1, wherein the decision feedback equalizer is a multiple decision feedback equalizer.

4. (original) The method of claim 1, wherein the decision feedback equalizer and symbol decoder are formed as an integrated block for passing data therebetween.

5. (original) The method of claim 1, wherein the symbol decoder is a Viterbi decoder, and wherein the Viterbi decoder computes intermediate decisions, select signals, and path select signals, and provides the decisions and signals to the decision feedback equalizer.

6. (currently amended) The method of claim 5, wherein the decision feedback equalizer is a multiple decision feedback equalizer, and wherein the multiple decision feedback equalizer computes ~~a plurality of possible~~ candidates for inputs to the Viterbi decoder, and selects decisions from the candidates and provides the selected inputs to the Viterbi decoder.

7. (currently amended) The method of claim 6, further including receiving outputs from the Viterbi decoder at the multiple decision feedback equalizer, using the Viterbi outputs to select Viterbi inputs from the set of ~~possible~~ values, providing the Viterbi inputs to the Viterbi decoder, and computing decisions and path select signals for a next symbol period at the Viterbi decoder.

8. (original) The method of claim 1, further including performing slicing functions at the decision feedback equalizer to produce the intermediate decisions, select signals and path select signals.

9-10. (cancelled)

11. (currently amended) A multiple decision feedback equalizer operable to cooperate with a symbol decoder to provide a next-cycle input sample from the decision feedback equalizer to the symbol decoder ~~using look-ahead computations~~, comprising:

circuitry operable to receive intermediate decisions and select signals from the ~~Viterbi~~ symbol decoder, compute a plurality of possible values for next-cycle decoder inputs and select a next-cycle input sample based on the select signals; and

an output circuit coupled to the circuitry to provide plural outputs to be delivered to the symbol decoder, wherein the respective outputs are buffered by delay elements.

12-15. (cancelled)